## REMARKS

Claims 1-15 are pending in this application. Claim 2 is cancelled without prejudice or waiver, and claims 1, 3 and 7-9 are amended herein. The changes to the amended claims are shown in the Appendix hereto, as required by 37 C.F.R. §1.121, with deletions indicated by bracketing and additions indicated by underlining.

Claims 7-9 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particular point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner points to claims 7-9, lines 2-3, as lacking antecedent basis for the term "the temperature". Claims 7-9 are amended herein to make clear that the temperature to which reference is being made is the temperature at which heating is being performed prior to the curing process. In addition, other changes to claims 7-9 are made herein to improve that clarity of the claim language. Accordingly, it is respectfully requested that the rejection by the Examiner on these claims under §112, second paragraph, be reconsidered and withdrawn.

Claims 1, 4, 14 and 15 stand rejected under 35 USC §102(e) as being anticipated by Willie et al., U.S. Patent No. 6,083,819. Except to the extent addressed by the amendments herein to claim 1, the rejection is respectfully traversed.

With regard to claim 1, the Examiner points to Willie as teaching a method of manufacturing a semiconductor device (Figs. 1-4, item 10; column 2, line 27), when a wafer (Figs. 1-4, item 12; column 2, line 26) having a main surface (Figs. 3-4, item 14; column 3, line 4), on which a plurality of bumps (Figs. 3-4, item 18; column 3, line 14), respectively connected to a plurality of electrode pads (Figs. 3-4, items 24 and 25; column 3, line 13), is brought into a resin molded type package (a standard practice in the art); placing a sheet of encapsulating material, item 19; column 3, line 20) containing a thermosetting resin over said wafer (item 12; column 3, line 19) so as to cover said main surface; and heating and curing said sheet encapsulating material by heating apparatus to form an encapsulating resin layer (Fig. 4, item 20; column 3, line 32).

It is respectfully submitted that the elements identified by the Examiner in Willie do not correspond to the features of the present invention. While the present invention was directed to a method of fabricating semiconductor devices involving encapsulation of an entire semiconductor wafer before the wafer is divided into individual chips, Willie discloses a method providing encapsulating between a semiconductor chip and the circuit board to which it is already mounted. For example, what the Examiner refers to as a wafer (item 12 in the figures) is, in fact, described at column 2, line 26, as a printed circuit board that is effective in receiving an integrated circuit die 16 to form the microelectronic assembly 10, shown in the figures. Willie fails to disclose a semiconductor wafer on a main surface of which are formed a plurality of semiconductor devices, as amended claim 1 requires.

As noted above, Willie discloses a process in which an encapsulant is disposed between the integrated circuit die and the printed circuit board after the integrated circuit is mounted to the printed circuit board (see generally, Willie column 2, lines 3-23). The encapsulant in Willie is not disposed by placing a sheet encapsulating material containing a thermosetting resin so as to cover the main surface of the semiconductor wafer, as claim 1 requires. Rather, Willie discloses that the encapsulant precursor 19 is placed on the printed circuit board around the periphery of the integrated circuit die, as shown in Fig. 3, and is subsequently heated to cause it to flow between the integrated circuit die 16 and the circuit board 12 into gap 30 due to capillary forces, which draw the precursor 19 under the integrated circuit die 16, as shown in Figure 4 (see generally column 3, lines 19-48). It would appear to be difficult, if not impossible, in Willie to interpose encapsulating material in the form of a sheet, between the integrated circuit die and the printed circuit board to which it is mounted.

Claim 1, as amended, includes two additional steps that originally appeared in claims 2 and 3. The first such step, originally in claim 2, is polishing and the encapsulating resin layer to expose portions of the plurality of bumps that are formed on the main surface of the semiconductor wafer. Willie does not disclose such a polishing process, nor would it appear possible to carry out a polishing process on the encapsulant of Willie after it has been cured in place between the integrated circuit die and the circuit board to which the die is connected.

The other step added by amendment to claim 1 is dividing the semiconductor wafer into individual semiconductor device chips. Willie does not disclose this step at all, because, as noted above, printed circuit board 12 is not a semiconductor wafer containing a plurality of semiconductor devices that would be divided into individual chips.

Hence, it is respectfully submitted that claim 1, as well as its dependencies, patentably distinguish over Willie.

Regarding claim 4, the Examiner points to Willie as teaching a method of manufacturing a semiconductor device, and disclosing that heating and curing are done by heating the wafer (figure 4, item 12) with the heating apparatus after the provision of sheet encapsulating material (item 19) over said wafer (column 3, lines 31-48). While the text referenced by the Examiner does disclose the method by which the encapsulating material is put in place between the printed circuit board 12 and the integrated circuit die 16, Willie fails to disclose that a sheet of encapsulating material is placed over the semiconductor wafer prior to heating and curing, as claim 4 requires. Rather, what Willie discloses, as noted above, is that the encapsulant precursor 19 is placed around the periphery of the integrated circuit die and the assembly subsequently heated to cause the precursor to flow under the die.

Regarding claim 14, the Examiner points to Willie as disclosing that the sheet encapsulating material (Fig. 3, item 19; column 3, line 20) contains a curing agent for curing thermosetting resin (epoxy resin + amine catalyst + filler silica or alumina), in a state in which the curing agent is enclosed in a capsule (Figs. 3-4, item 19; column 3, line 23) broken at curing temperature to form encapsulant 20 (Fig. 4, item 20; column 3, line 32). What the figures and text referenced by the Examiner disclose is that the precursor 19 is dispensed on the printed circuit board around the periphery of the integrated circuit die 16 as a single component, preferably using a syringe. Contrary to the Examiner's position, there is no suggestion of a capsule containing a curing agent, which capsule breaks at curing temperature to enable the encapsulating material to cure. Unlike the present invention, in which the encapsulating material in the form of a sheet is placed over the surface of the semiconductor wafer, it would not seem possible, and the Examiner fails to explain how, a capsule containing a curing agent would be

integrated into the method used in Willie to dispense the precursor.

Regarding claim 15, the Examiner points to Willie as disclosing that the sheet encapsulating material (Figs 3-4, item 20; column 3, line 23) contains an antifoaming agent (amine catalyst + filler silica or alumina), for removing voids contained in the sheet encapsulating material (column 3, lines 19-48). Contrary to the Examiner's position, nothing in the referenced text or figures suggests that any of the components of precursor 19 functions as an antifoaming agent, nor does Willie discussed at all the subject of removal of voids.

Hence, for the foregoing reasons, is respectfully submitted that claims 4, 14 and 15 independently distinguish over Willie.

Claims 2 and 5 stand rejected under 35 U.S.C. §103(a) as being obvious over Willie in view of King et al., U.S. Patent No. 6,232,213 B-1. The rejection is respectfully traversed.

With respect to claim 2, the Examiner acknowledges that Willie fails to show the step of polishing the encapsulating resin layer to thereby expose the tops of the bumps formed on the surface of the semiconductor wafer, after forming the encapsulating resin layer. However, the Examiner points to King as disclosing the step of polishing an encapsulating resin layer (Fig. 7, item 26; column 4, line 47) to thereby expose the tops of bumps (Fig. 7, item 34; column 4, line 50) after forming an encapsulating resin layer (see King column 4, lines 46-56 ).

Contrary to the Examiner's position, what the referenced figures and text disclose is that the encapsulating material in King is formed with openings 30 to expose conductive leads 12 at the bond area 34. Openings 30 are sized and shaped according to the size and shape of solder balls 38, which formed the external electrodes. Any resin residue that is present on the bond area after capsulation is removed by electrolytic or mechanical deflash processes well known in the art. Hence, King does not disclose polishing the encapsulating resin layer to expose the tops of bumps formed on the semiconductor wafer below, as required by claim 2, which has been incorporated by the amendments herein into claim 1. At most, King discloses a process for removing residue from holes already formed during the encapsulating process, but it is not taught or suggested in King that such process involves polishing the surface of the

encapsulating resin layer. Moreover, as has been discussed above, one can only question what would motivate one of ordinary skill in the art to apply any polishing technique at all to the encapsulating layer in Willie that is between the integrated circuit die and the printed circuit board to which it is already attached, if the purpose of the polishing process is to expose bumps for subsequent electrical connection. Hence, it is respectfully submitted that the limitation of claim 2, which now appears in claim 1, patentably distinguishes over the applied art combination of Willie and King.

The Examiner's rejection of claim 5 relies only on Willie, and not on King. Accordingly, for at least the reasons discussed above the connection with claim 1, it is respectfully submitted that claim 5 also distinguishes over the applied art.

Claims 3, 6, 10, 11, 12 and 13 stand rejected under 35 U.S.C. §103(a) as being obvious over Willie in view of Applicant's Admitted Prior Art (AAPA). The rejection is respectfully traversed.

The Examiner's rejection of each of dependent claims 3, 6, 10, 11, 12 and 13 begins with the premise that Willie teaches a method of manufacturing semiconductor device. However, Figs. 1-4, item 10 and column 2, line 27, referenced by the Examiner, disclose the printed circuit board 12 that is effective in receiving integrated circuit die 16 to form a microelectronic assembly 10. Willie, as discussed above, does not disclose the method of the present invention in which a semiconductor wafer is first encapsulating and then divided into individual semiconductor device chips. Hence, the reasons discussed above in connection with claim 1, is respectfully submitted that dependent claims 3, 6, 10, 11, 12 and 13 patentably distinguish over the applied art references. Further, it is respectfully submitted that these rejected claims recite features that independently distinguish over Willie and the AAPA.

For example, with respect to claims 3, the Examiner acknowledges that Willie fails to show forming external terminals each having conductivity so as to be connected to the bumps respectively. To cure this defect in Willie, the Examiner points to the AAPA as disclosing the formation of external terminals (Application Fig. 8(E), item 72, page 2, line 18) each having conductivity so as to be connected to the bumps (Fig. 8(E), item 70; page 2, line 19) respectively. However, the prior art references provide no motivation for one of ordinary skill in the art to make the combination proposed by the

Examiner. Willie fails to disclose or suggested how any external terminals would be applied to the microelectronic assembly 10. The only terminals shown in Willie are internal to the assembly, i.e., solder balls 18 that connect bond pads 24 and 25 on the printed circuit board and integrated circuit die, respectively.

With regard to claim 10, the Examiner points to Willie as disclosing that the covering by the sheet of encapsulating material (Figure 3, item 19; column 3, line 19) is carried out by successively placing the sheet encapsulating material over the wafer (item 12) from the end of the sheet encapsulating material, so it is inherent as shown by the AAPA (Application page 2, lines 1-11) that in such a process air is expelled. As noted above, Willie fails to disclose that encapsulating material in the form of a sheet is applied in any manner to either the printed circuit board or the integrated circuit die. Moreover, the section of the application referenced by the Examiner discloses a process whereby a quantity of encapsulating resin is caused to spread out over the surface of the semiconductor wafer by pressure applied in a press. Hence, neither of the references, nor the combination of the two, teach or suggest the claimed invention, as claimed in claim 10.

With respect to claims 12 and 13, the Examiner acknowledges that Willie fails to disclose that the external terminals are formed after formation of a wiring metal over the sheet encapsulating material, or that the external terminals are formed in place of the bumps. To cure this defect in Willie, Examiner points to the AAPA as disclosing that the external terminals are formed after formation of a wiring metal over the sheet encapsulating material (Application Fig. 8(A), item 68; page 2, line 6), and are formed in place of bumps. It is respectfully submitted that the text referenced by the Examiner in the application fails to disclose the features recited in claims 12 and 13. The referenced text discusses only the application of external terminals to bumps that are exposed after encapsulation of the semiconductor wafer in a press according to the AAPA.

Accordingly, it is respectfully submitted that this application, as amended, is in condition for allowance. Such action, and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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## APPENDIX

## AMENDED CLAIMS

**(With deletions in brackets and additions underlined)**

1. (Amended) A method of manufacturing [a] semiconductor [device, when a wafer having a main surface on which a plurality of bumps respectively connected to a plurality of electrode pads are formed, is brought into a resin molded type package to thereby manufacture said semiconductor device] devices, comprising:

forming a plurality of semiconductor devices on a main surface of a semiconductor wafer, the plurality of semiconductors having a plurality of electrode pads for respectively connecting thereto;

forming a plurality of bumps on said main surface that are respectively connected to said electrode pads;

placing a sheet of encapsulating material containing a thermosetting resin having a curing temperature over said semiconductor wafer so as to cover said main surface; [and]

heating and curing said sheet encapsulating material by a heating apparatus to thereby form an encapsulating resin layer[.];

polishing said encapsulating resin layer to expose portions of said plurality of bumps; and

dividing said semiconductor wafer into individual semiconductor device chips.

3. (Amended) The method as claimed in claim 1, further comprising:

forming external terminals each having conductivity so as to be connected to said bumps respectively. [; and]

[cutting said wafer in which the formation of said external terminals has been finished, into each individual chips.]

7. (Amended) The method as claimed in claim 1, wherein said heating and curing are done in such a manner that the heating [temperature] of said sheet encapsulating material is [taken as] at a temperature lower than the curing temperature of said sheet

encapsulating material, and at which the viscosity of said sheet encapsulating material is kept low, and said sheet encapsulating material is kept for a predetermined time at a temperature at which voids contained in said sheet encapsulating material are easy to be eliminated, and thereafter [the temperature of] said sheet encapsulating material is increased in temperature to said curing temperature or higher.

8. (Amended) The method as claimed in claim 1, wherein said heating and curing are done in such a manner that the heating [temperature] of said sheet encapsulating material is [taken as] at a temperature lower than the curing temperature of said sheet encapsulating material, and at which the viscosity of said sheet encapsulated material is kept low, and said sheet encapsulating material is kept for a predetermined time at a reduced pressure at a temperature at which voids contained in said sheet encapsulating material is easy to be eliminated, and thereafter [the temperature of] said sheet encapsulating material is increased in temperature to said curing temperature or higher.

9. (Amended) The method as claimed in claim 1, wherein said heating and curing are done in such a manner that the heating [temperature] of said sheet encapsulated material is [taken as] at a temperature lower than the curing temperature of said sheet encapsulating material, and at which the viscosity of said sheet encapsulating material is kept low, and said sheet encapsulated material is kept for a first predetermined time under a first reduced pressure at a void removal temperature at which voids contained in said sheet encapsulating material are easy to be eliminated, and thereafter repeatedly held plural times for a second predetermined time while being kept at the void removal temperature [under] at a second reduced pressure between [a pressure value placed under] the first reduced pressure and [a pressure value of] atmospheric pressure, and thereafter [the temperature of] said sheet encapsulated material is increased in temperature to the curing temperature or higher.